Notice of Allowability	Application No.	Applicant(s)
	10/776,938	TALWAR ET AL.
	Examiner	Art Unit
	Krista M. Flanagan	2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment and response filed on 28 November 2005*.

2. ☒ The allowed claim(s) is/are *1-52*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Timothy B. Clise on 05 December 2005.

The application has been amended as follows:

- Claim 30 has been amended to provide the correct gate information. It has been amended from "A logic circuit according to claim 28, wherein said second combining logic comprises an $((A+B)(C+D))^C$ gate to implement the logic equation $((A+B)(C+D))^C$, wherein + denotes logical OR, proximity denotes logical AND, ^{C} denotes complements and A, B, C, D denote inputs to said $((A+B)(C+D))^C$ gate." To now read -A logic circuit according to claim 28, wherein said second combining logic comprises an $(AB+CD)^C$ gate to implement the logic equation $(AB+CD)^C$, wherein + denotes logical OR, proximity denotes logical AND, ^{C} denotes complements and A, B, C, D denote inputs to said $(AB+CD)^C$ gate.-

REASONS FOR ALLOWANCE

2. The following is an examiner's statement of reasons for allowance:

a. Regarding claim 1, prior art fails to disclose a logic circuit comprising two logic levels, the first level logic comprising two logic parts, each logic part comprising a NOR gate and a NAND gate and having two first level inputs for receiving the binary inputs and two first level outputs and the second level logic comprising four second level

outputs, four second level inputs for receiving second level binary inputs and connected to the four first level outputs, a NAND gate, a first gate generating a logical OR combination of two second level binary inputs and NAND combining the logical OR combination with two other second level binary inputs, a second gate generating logical OR combinations of two pairs of second level binary inputs and NAND combining the logical OR combinations, and a NOR gate where NAND and NOR combining is used to save silicon space and to provide faster processing.

b. Regarding claim 5, prior art fails to disclose a logic circuit comprising two logic levels, the first level logic comprising two logic parts, each logic part comprising a NOR gate and a NAND gate and having two first level inputs for receiving the binary inputs and two first level outputs and the second level logic comprising four second level outputs, four second level inputs for receiving second level binary inputs and connected to the four first level outputs, a NAND gate, a first gate generating logical AND combinations of two pairs of second level binary inputs and NOR combining the logical AND combinations, a second gate generating logical OR combinations of two pairs of second level binary inputs and NAND combining the logical OR combinations, and a NOR gate where NAND and NOR combining is used to save silicon space and to provide faster processing.

c. Regarding claim 9, prior art fails to disclose a logic circuit comprising two logic levels, the first level logic comprising two logic parts, a first logic part comprising a NOR gate and a NAND gate and having two first level inputs for receiving two of the binary inputs and two first level outputs, and a second logic part comprising an inverter having

one first level logic input for receiving one of the binary inputs and one first level output and the second level logic comprising three second level outputs, and three second level inputs for receiving second level binary inputs and connected to the three first level outputs, a NAND gate, a gate generating a logical AND combination of two second level binary inputs and NOR combining the logical AND combination with one other second level binary input, and a NOR gate where NAND and NOR combining is used to save silicon space and to provide faster processing.

d. Regarding claim 12, prior art fails to disclose a logic circuit comprising: first level logic comprising two logic parts, a first logic part comprising a NOR gate and a NAND gate and having two first level inputs for receiving two of the binary inputs and two first level outputs, and a second logic part comprising an inverter having one first level logic input for receiving one of the binary inputs and one first level output and the second level logic comprising three second level outputs, and three second level inputs for receiving second level binary inputs and connected to the three first level outputs, a NAND gate, a gate generating a logical OR combination of two second level binary inputs and NAND combining the logical OR combination with one other second level binary input, and a NOR gate where NAND and NOR combining is used to save silicon space and to provide faster processing.

e. Regarding claim 15, prior art fails to disclose a logic circuit having seven binary inputs, the logic circuit comprising: first logic for generating a first binary value as a threshold function which is high if at least four binary inputs are high, a second binary value as a threshold function which is high if less than two binary inputs are high, and a

third binary value as a threshold function which is high if less than six binary inputs are high; and second logic for forming the OR combination of the first binary value and the second binary value and for NAND combining the third binary value and the result of the OR combination where NAND combining is used to save silicon space and to provide faster processing.

f. Regarding claim 34, prior art fails to disclose a logic circuit having seven binary inputs, the logic circuit comprising: first logic for generating a first binary value as a threshold function which is high if at least four binary inputs are high, a second binary value as a threshold function which is high if less than two binary inputs are high, and a third binary value as a threshold function which is high if less than six binary inputs are high; and an inverting multiplexer to select and output the inverse of the second or third binary value dependant upon the first binary value where NOR combining is used to save silicon space and to provide faster processing..

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Krista M. Flanagan whose telephone number is (571) 272-2203. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Flanagan
20051205

Robert Pascal
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